REMARKS

The Office Action dated April 7, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Currently, claims 2-10 have been allowed and claims 11-35 have been withdrawn from consideration. By this Amendment, claims 1, 36 and 43 have been amended to more particularly point out and disclose the claimed invention. The claims have been amended to provide proper antecedent basis for claim terminology. Therefore, the amendments are merely cosmetic in nature. Claims 44-46 have been cancelled. No new matter has been added or amendments made that narrow the scope of any elements of any claims. Accordingly, claims 1-10 and 36-43 are pending in this application and are submitted for consideration.

Claims 1 and 37-24[1] were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. By this amendment, claims 1, 36 and 43 have been further amended. Claims 44-46 have been cancelled, rendering them moot with regard to this rejection. Therefore, the rejection is requested to be withdrawn.

Claims 1 and 36-46 were rejected under 35 U.S.C. § 102(e) as being anticipated by Okutsu et al. (U.S. Patent No. 6,433,623, "Okutsu"). In making this rejection, the Office Action took the position that Okutsu discloses all the elements of the claimed invention. By this amendment, claims 44-46 have been cancelled, rendering them moot with regard to this rejection.

[1] It appears the Examiner meant to say the claims 1 and 36-46 are rejected under 35 U.S.C. § 112, second paragraph.

However, Applicants respectfully submit that claims 1 and 36-43 recite subject matter that is neither disclosed nor suggested in Okutsu.

Applicants' amended claim 1 recites a level shift circuit that includes a capacitor and a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. The limiting circuit limits the voltage provided to the capacitor when boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Applicants' amended claim 36 recites a level shift circuit including a capacitor and a first transistor connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A second transistor is connected to the high potential power supply and the first transistor for being turned off before the first transistor is turned off when boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Applicants' amended claim 43 recites a level shift circuit including a capacitor and a charge control circuit connected to the capacitor, for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit, for limiting the voltage provided to the capacitor from the high potential power

supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. The limiting circuit limits the voltage provided to the capacitor when charging of the capacitor to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

In making this rejection, the Office Action took the position that Okutsu discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the shift level circuit of the present invention includes a capacitor and a charge control circuit connected to the capacitor that provides a voltage of a high potential power supply to the capacitor and also controls the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

As a result of this claimed configuration, when the capacitor performs voltage step-up, the current limiting circuit limits the charge that leaks from the capacitor to the high potential power supply and increases the voltage step-up efficiency. This improves the response of the output signal in the level shift circuit.

The present invention is directed to a level shift circuit that includes a limiting circuit connected to a high potential power supply and a charge control circuit. The limiting circuit limits the voltage provided to a capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential

power supply to the capacitor. That is, the limiting circuit is turned off before the charge control circuit is turned off.

Okutsu discloses a voltage boosting circuit that includes a capacitor C1 connected between power supply terminal 1 and output terminal 2. Control circuit 14 is connected to clock signal input terminal 3. Charge transfer circuit 6 is connected between capacitor C1 and output terminal 2. Bias circuit 11 is connected between power supply terminal 1 and output terminal 2. Switching circuits 12 and 13 are connected between power supply terminal 1 and node 9.

With respect to claims 1 and 43, the Office Action asserted that in Fig. 1, Okutsu discloses limiting circuit P12 for limiting a voltage provided to capacitor C1 from a high potential power supply before charge control circuit P13 stops providing the voltage of the high potential power supply to the capacitor, and that limiting circuit P12 limits the voltage provided to the capacitor C1 when the boosting of an output signal at node 9. However, Applicants respectfully disagree. Okutsu does not appear to disclose that the limiting circuit limits providing a voltage before the charge control circuit is operated. As a matter of fact, in Okutsu, it appears that the PMOS transistor P12 and the PMOS transistor P13 are simultaneously turned off when boosting of an output signal is started.

As shown in Fig. 1, and discussed in columns 9 and 10 of Okutsu, the PMOS transistor P12 is turned off when an inverter G13 provides the gate of the PMOS transistor P12 with a high output voltage by receiving a low input voltage. The PMOS transistor P13 is turned off when an inverter NMOS transistor N3 and PMOS transistor P14 provides the gate of the PMOS transistor P13 with a high output voltage by

receiving a low input voltage that is lower than a voltage at a node 9 (power supply voltage VCC or boosted voltage). Therefore, when a node T2, which is connected to the inverters G13, NMOS transistor N3 and PMOS transistor P14, is set to a low voltage, the PMOS transistor P12 and the PMOS transistor P13 are simultaneously turned off (see column 9, line 60 to column 10, line 12 of Okutsu).

Therefore, Okutsu fails to disclose or suggest a level shift circuit having a limiting circuit connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor, as recited in Applicants' amended claims 1 and 43. Okutsu also fails to disclose or suggest that the limiting circuit limits the voltage provided to the capacitor when boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started, as further recited in Applicants' amended claim 1. Additionally, Okutsu fails to disclose or suggest that the limiting circuit limits the voltage provided to the capacitor when charging of the capacitor to a boosted voltage, which is higher than the voltage of the high potential power supply, is started, as further recited in Applicants' amended claim 43.

Applicants' amended Claim 36 of the present invention further recites that the level shift circuit includes a second transistor connected to the high potential power supply and the first transistor, which is turned off before the first transistor is turned off when boosting of an output signal of a level shift circuit to a boosted voltage is started.

However, Okutsu fails to suggest this limitation. As discussed above, in Okutsu, the first transistor (PMOS transistor P12) and second transistor (the PMOS transistor P13) are simultaneously turned off.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claims 1, 36 and 43, is not anticipated within the meaning of 35 U.S.C. § 102.

As claims 37-39 depend directly or indirectly from claim 36 and claims 40-42 depend directly or indirectly from claim 1, Applicants respectfully submit that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least same reasons as discussed above.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1 and 36-43, (claims 2-10 already being allowed) and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-00054.**

Respectfully submitted,
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Enclosures: Petition for Extension of Time

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